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(19)

(54) IMPROVEMENTS IN OR RELATING TO DATA TRANSMISSION SYSTEMS

(71) We, STANDARD TELEPHONES AND CABLES LIMITED, a British Company, of 190 Strand, London, W.C.2, England, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to data transmission systems in which error detection and correction facilities are provided.

According to the present invention there is provided a data transmission system, in which full duplex principles are used, i.e. separate GO and RETURN channels are provided, in which the detection of an error in either of said directions causes retransmission cycles in both directions, in which the signals sent from a receiving device to a transmitting device to indicate correct reception (OK) or a request for retransmission (RQ) of an incorrectly-received data block are included in data blocks so as to be protected by the error detection facilities of the system, in which the transmission cycle used for the error correction consists of N blocks from each of said terminals, in which the transmitted blocks are sequentially numbered with the numbers running from 1 up to (N+1), i.e. the number of blocks in the cycle of sequence numbers is one greater than the number of blocks in the retransmission cycle used for error correction, which sequence of numbers is cyclically repeated throughout transmission, in which during normal operation wherein transmission and reception are error-free, the block numbers are not transmitted, and in which when an error is detected one or more block numbers are sent on resumption of correct transmission, thus ensuring that blocks are sent to an utilization output in the correct order.

An embodiment of the invention will now be described with reference to the drawings, in which Figure 1 shows explanatory diagrams relating to data transmission, while Figure 2 is a simplified block diagram.

In such a system it may be found that transmission of the block number is not always necessary, in which case the block numbers are not transmitted during normal operation or when an EDC retransmission cycle is in progress, these numbers only being sent when resynchronisation of the two terminals has to take place. Such resynchronisation is needed when due to a prolonged fault, block synchronisation has been lost. In such case the sequence number of at least the first block is sent after resynchronisation.

It is assumed that both directions of transmission are slaved to the same clock, so that although the relative phase of the transmitted and received blocks at a terminal is arbitrary, it remains constant.

The blocks considered herein consist of a number of data bits, followed by service bits (if any), followed by parity bits. Acknowledgement signals are conveyed by parity bits and/or service bits, not by data bits. Thus at the conclusion of a received block its acknowledgement can be included in the block then being sent from the receiving station, provided that the service and parity bits have not been reached. Here it is assumed that where service bits are used, one only is needed to indicate the reception of a corrupt block and the start of a retransmission cycle. If we assume zero propagation time, and that a block sent from terminal X to terminal Y commences at time $t=0$, the earliest time at which the return block with the corresponding acknowledgement can end is (2T—U) and the latest time is (3T—U), where T is the duration of a block and U is the duration of the data bits in a block. Such an acknowledgement is available at X *before* the transmission of the third block from X to Y has been completed. If we consider the effect of a finite propagation time, the above still holds as long as the loop propagation time does not exceed U.

Thus with a bit rate of 48k bits, and a block with 240 data bits, the limiting loop propagating time is 5 ms, which corresponds to a circuit length of 250 miles at 100 miles per millisecond. Thus it can normally be

assumed that the acknowledgement of block 1 from X is available at X before the end of transmission of block 3, and can then determine what follows block 3. The acknowledgement may in fact be available before the end of block 2, in which case it can be stored until block 3.

Transmission in the two directions can be represented as follows:

(a) Terminal X to Terminal Y X1 X2 X3
(b) Terminal Y to Terminal X Y1 Y2 Y3

in which case the acknowledgement of X1 can be conveyed by Y2, and that of Y1 by X3.

We now consider an "RQ system" with a repeat cycle of three blocks, operating as follows:

(I) on receipt of an uncorrupted block *with an OK signal*, normal sequential transmission continues

(II) on receipt of an uncorrupted block *with an RQ signal*, the last three blocks are repeated in order, with an O.K. signal

(III) on receipt of a corrupt block, repeat the last three blocks with the first of them carrying an RQ signal

(IV) on receipt of a corrupt block or of a block with an RQ signal, discard that block and also the two following blocks, *with* their OK or RQ signals.

One critical error condition is that where three consecutive blocks in one direction are corrupted. The occurrence of a single corrupted block in various relative positions in the reverse direction is now considered, see Figure 1, where blocks sent on to the utilization output are underlined, and blocks corrupted in transmission are crossed out with a diagonal line. Figure 1*a* relates to the case with no corruptions in the direction Y to X, Figure 1*b* when block Y4 is corrupted, Figure 1*c* when block Y3 is corrupted and Figure 1*d* where block Y2 is corrupted. In Figures 1*a*, 1*b* and 1*c*, correct sequences of data blocks pass to the utilization outputs, but in Figure 1*d*, Y receives X1, X2 and X3 twice, while X does not even receive Y2, Y3 and Y4. Further, as shown, Y is unable to distinguish between (a) and (b): in both cases all that Y "knows" is that three blocks which follow X3 were corrupted.

This is resolved in the present system by sequential numbering (which in this context includes lettering) the blocks in a cycle which is one more than the number of blocks in the repeat cycle, i.e. 4. The criteria for passing a block to the utilization output are that it is uncorrupted, and that it has the next number (or letter) in the sequence. Thus if X1 and X5 are labelled A, X2 and X6 labelled B, X3 and X7 are labelled C, and X4 and X8 labelled D, then the correct block sequences reach the outputs. This sequencing will require two extra service bits, the OK/RQ bit being retained to ensure that perpetual repetitions in both directions do not occur.

In some cases such a situation as Figure 1*d* may not occur and normal operation, or a normal EDC retransmission cycle may be possible without use of the sequence numbers. Where this applies, these sequence numbers, although continuously generated are only sent when the terminals have to be resynchronised. In such case the sequence number of at least the first block after the resynchronisation takes place is sent. Thus a simple RQ system, i.e. one with no sequence numbers, could be used for normal working, but sequence numbering added only when a prolonged line fault occurs. This allows block corruption to be used as an RQ signal, leaving a free choice of sequence numbering when used with the EDC equipment, or the terminal equipment, or with a communications processor in, for instance, a packet switched network.

Note that the use of sequence numbers could save transmission time in that it would allow stored non-corrupted blocks to be "sorted out" into the correct order.

Figure 2 shows schematically how the above method might operate, only those units directly relevant to the sequence numbering being shown. For fuller explanation of the complete system reference should be made to Patent Application No. 45218/73 (Serial No. 1,409,184). (See also Patent Application No. 48618/71, Serial No. 1,366,908).

The formation of blocks for transmission is under the control of the TX Timing Distributor 1. The Synch. and Start Control 2 in conjunction with the TX Retransmission unit 4 determines whether the information bits are fresh data (by opening G3), retransmitted data from the RTM data store (by opening G3), or synchronising or Start of Data blocks (by opening G2).

A sequence counter 3 is provided, which has a cycle one more than the number of blocks in a retransmission cycle. By means of control inputs to it from the TX timing distributor 1, the TX RTM unit 4 and Sync. and Start Control 2, it is possible to arrange that the counter steps only when data blocks are transmitted, and also that it is appropriately corrected, when a retransmission cycle takes place, so that its reading always corresponds with the serial number appropriate to the block about to be transmitted, and also that a particular data block always retains the same number, however many times it has to be retransmitted. Such an arrangement would be needed if sequence numbers were transmitted with each block.

In the example being described, it is assumed that, after completion of block synchronisation or resynchronisation, the first data block to be transmitted (or retransmitted in the case of resychronisation) is preceded

by a 'Start of Data' block, generated by the Sync. and Start Generator. The reading of the counter, announcing the serial number of the first data block to be transmitted or retransmitted can conveniently be conveyed by service bits, within the Start of Data block and allocated for the purpose. When the Sync. and Start Control 2 applies enabling polarity to its St output and thus causes the Sync. and Start Generator to generate a Start of Data block, it also opens gate G22 and causes the reading of the Sequence Counter to be inserted in the block.

A receive side sequence counter 5 is also provided. In normal data reception, gate G23 applies an input pulse to step this counter once for each data block passed to the data terminal. The reading of the counter 5 is continuously supplied to the Sync. and Start Control 2. On resynchronisation, when the Sync. and Start Control 2 receives a signal from the Sync. and Start Detector 6 indicating that a Start of Data block has been received, it also receives the sequence number contained in that block. Note that in this system, when resynchronisation is called for, a start of data block (also called return-to-data block) is sent once in each direction after resynchronisation has been effected. Such a service block is also sent after initial block synchronisation. From these two numbers, the control unit can determine when to apply enabling polarity to G7 and G23. Thus, for example, if the retransmission cycle is of three blocks, so that the sequence numbering cycle will be four, and if the Sequence Counter in the receiver indicates that the next data block required has serial number 1, whereas the Start of Data block received indicates that the sequence number of the first retransmitted data block will be 3, the Sync. and Start control 2 will not apply enabling potential to G7 and G23 for the first two OK data blocks received.

For initial synchronisation, it is not necessary to suppress any received OK data blocks, but it is necessary to ensure that the sequence counter is in step with that at the remote transmitter. By means of the control lead shown dotted between the Syn. and Start Control 2 and the sequence counter 5, brought into operation manually for initial synchronisation, the sequence counter reading is caused by overriding control to coincide with the sequence number contained in the received Start of Data block.

It is to be understood that the foregoing description of specific examples of this invention is made by way of example only and is not to be considered as a limitation on its scope.

WHAT WE CLAIM IS:—

1. A data transmission system, in which full duplex principles are used, i.e. separate GO and RETURN channels are provided, in which the detection of an error in either of said directions causes retransmission cycles in both directions, in which the signals sent from a receiving device to a transmitting device to indicate correct reception (OK) or a request for retransmission (RQ) of an incorrectly-received data block are included in data blocks so as to be protected by the error detection facilities of the system, in which the transmission cycle used for the error correction consists of N blocks from each of said terminals, in which the transmitted blocks are sequentially numbered with the numbers running from 1 up to (N+1), i.e. the number of blocks in the cycle of sequence numbers is one greater than the number of blocks in the retransmission cycle used for error correction, which sequence of numbers is cyclically repeated throughout transmission, in which during normal operation wherein transmission and reception are error-free, the block numbers are not transmitted, and in which when an error is detected one or more block numbers are sent on resumption of correct transmission, thus ensuring that blocks are sent to an utilization output in the correct order.

2. A data transmission system, in which full duplex principles are used, i.e. separate GO and RETURN channels are provided, in which the detection of an error in either of said directions causes retransmission cycles in both of said directions, in which the retransmission cycle used for error detection and correction consists of N blocks from each of the terminals, in which the blocks are sequentially numbered with the numbers running from 1 up to (N+1), continuously repeated, i.e. the number of blocks in the cycle of sequence numbers is one greater than the number of blocks in the retransmission cycle used for error correction, in which the said sequence numbers are not sent when transmission conditions are satisfactory, being held in temporary storage at the terminals, and in which when the system is recovering from a loss of block synchronisation the said sequence numbers are sent until the system is functioning satisfactorily.

3. A block-coded error detection and correction system for synchronous duplex digital circuits, in which during normal data transmission sequence numbers are not sent with each block, in which the transmitting and receiving terminals each have sequence number counters which step once for each data block sent and keep in step for each data block successfully sent, in which the first data block to be sent after initial synchronisation or after resynchronisation is conveyed to the remote receiver in a service block sent before that first data block, and in which the sequence number thus sent is used at the remote receiver to set its sequence counter

to the correct starting reading in the case of initial synchronisation, and to determine the first correctly-received data block to be passed to the terminal's utilization output in the case of resynchronisation.

4. A data transmission system, substantially as described with reference ot the accompanying drawings.

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Chartered Patent Agent,
For the Applicants.

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1 428 050
2 SHEETS

COMPLETE SPECIFICATION

This drawing is a reproduction of the Original on a reduced scale.

SHEET 1

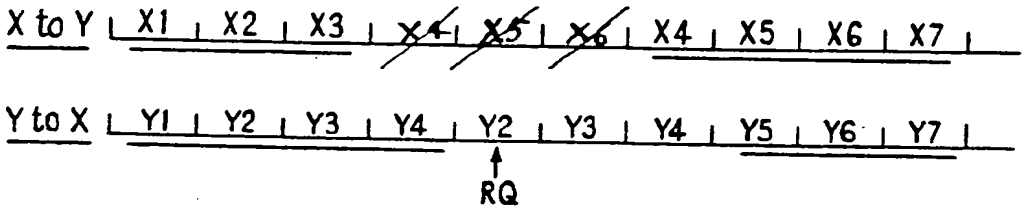

FIG.1a

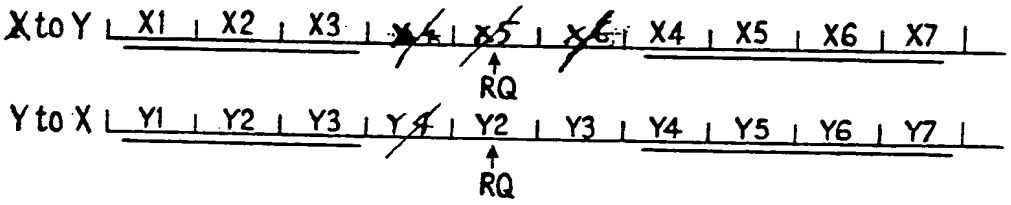

FIG.1b

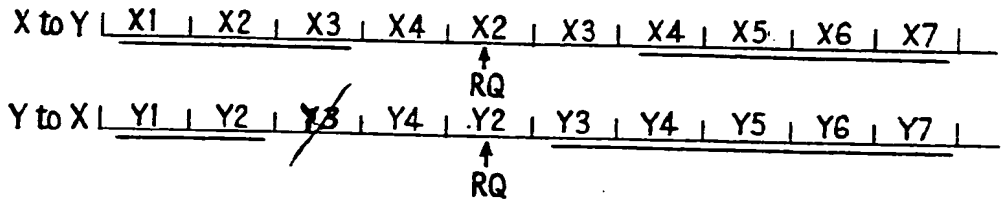

FIG.1c

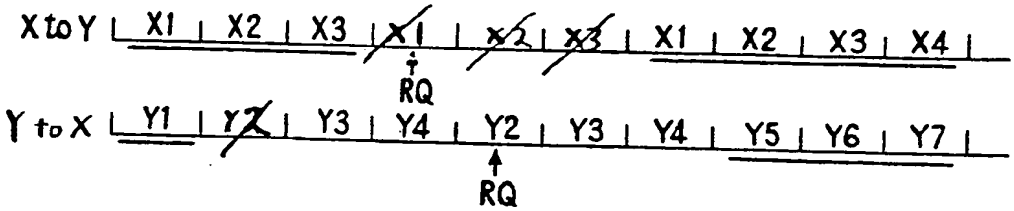

FIG.1d

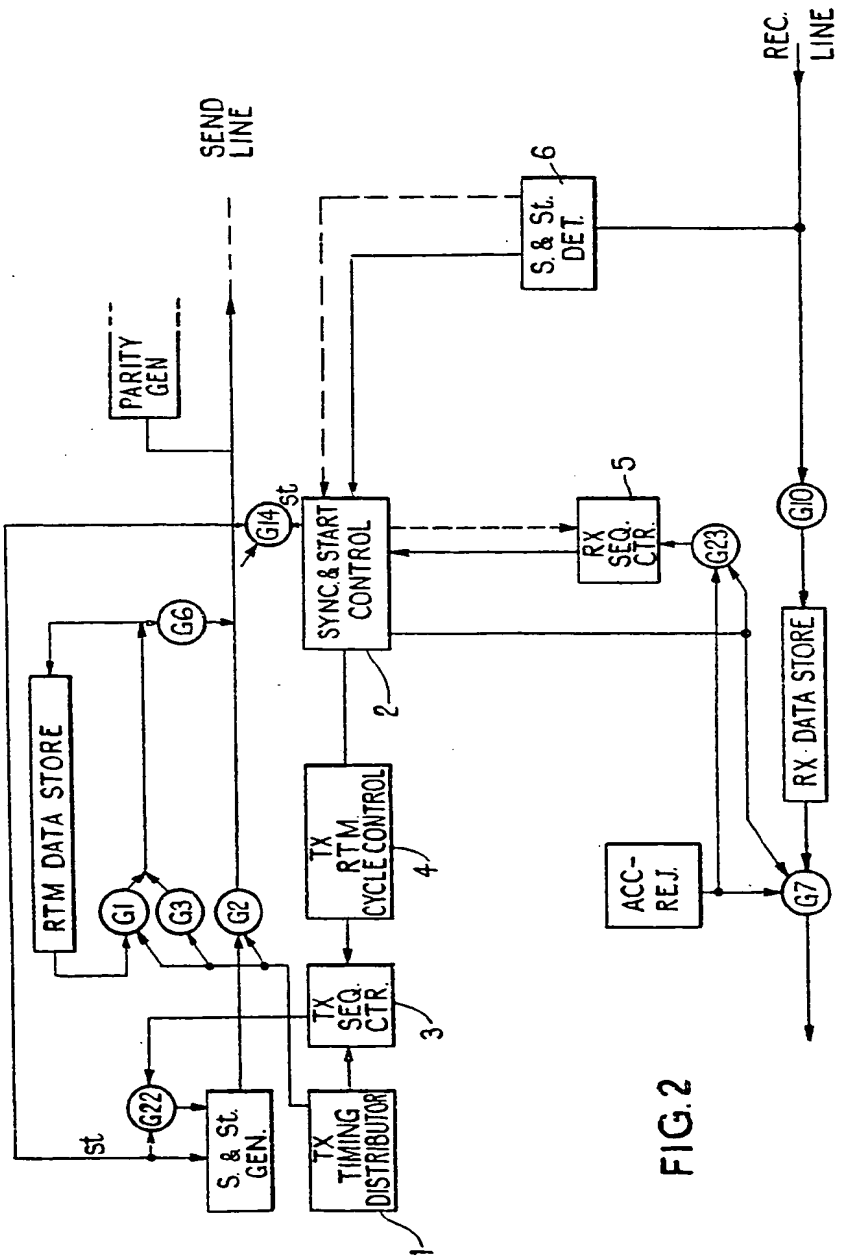
REC. LINE
SEND LINE
S. & St. DET.
6
PARITY GEN
SYNC. & START CONTROL
RX SEQ. CTR.
5
G10
G14
St
G23
G6
RTM DATA STORE
RX DATA STORE
2
TX RTM. CYCLE CONTROL
4
ACC-REJ.
G7
G1
G3
G2
TX SEQ. CTR.
3
G22
S. & St. GEN.
TX TIMING DISTRIBUTOR
1
st

FIG. 2

1 428 050
2 SHEETS

COMPLETE SPECIFICATION

SHEET 1

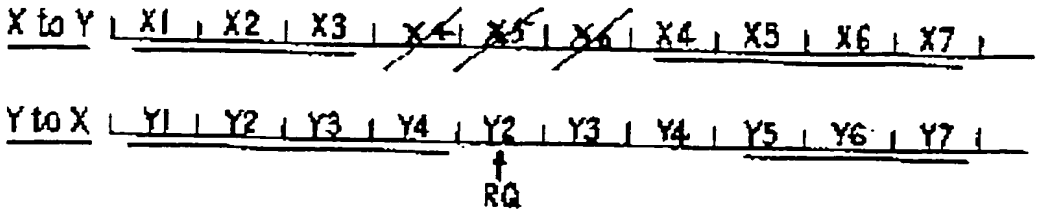

FIG.1a

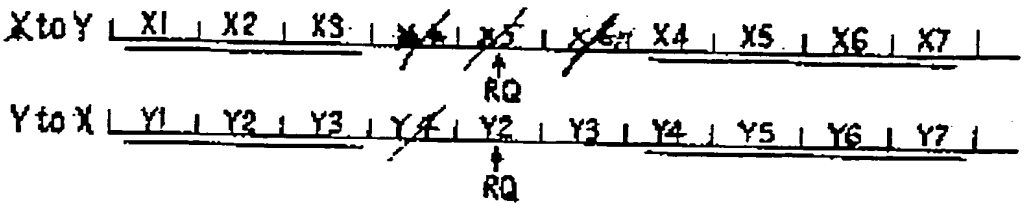

FIG.1b

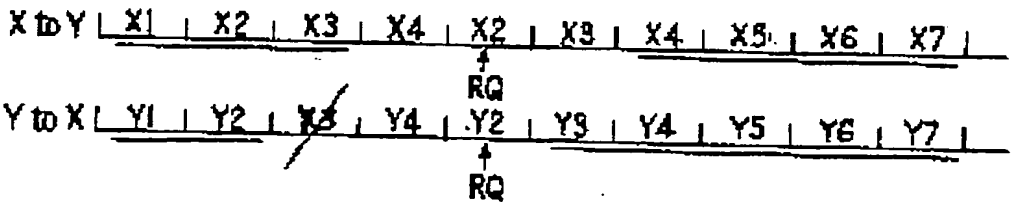

FIG.1c

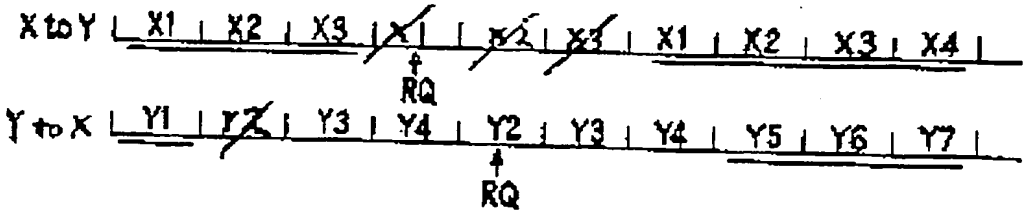

FIG.1d

1 428 050 COMPLETE SPECIFICATION
2 SHEETS
This drawing is a reproduction of the Original on a reduced scale.
SHEET 2

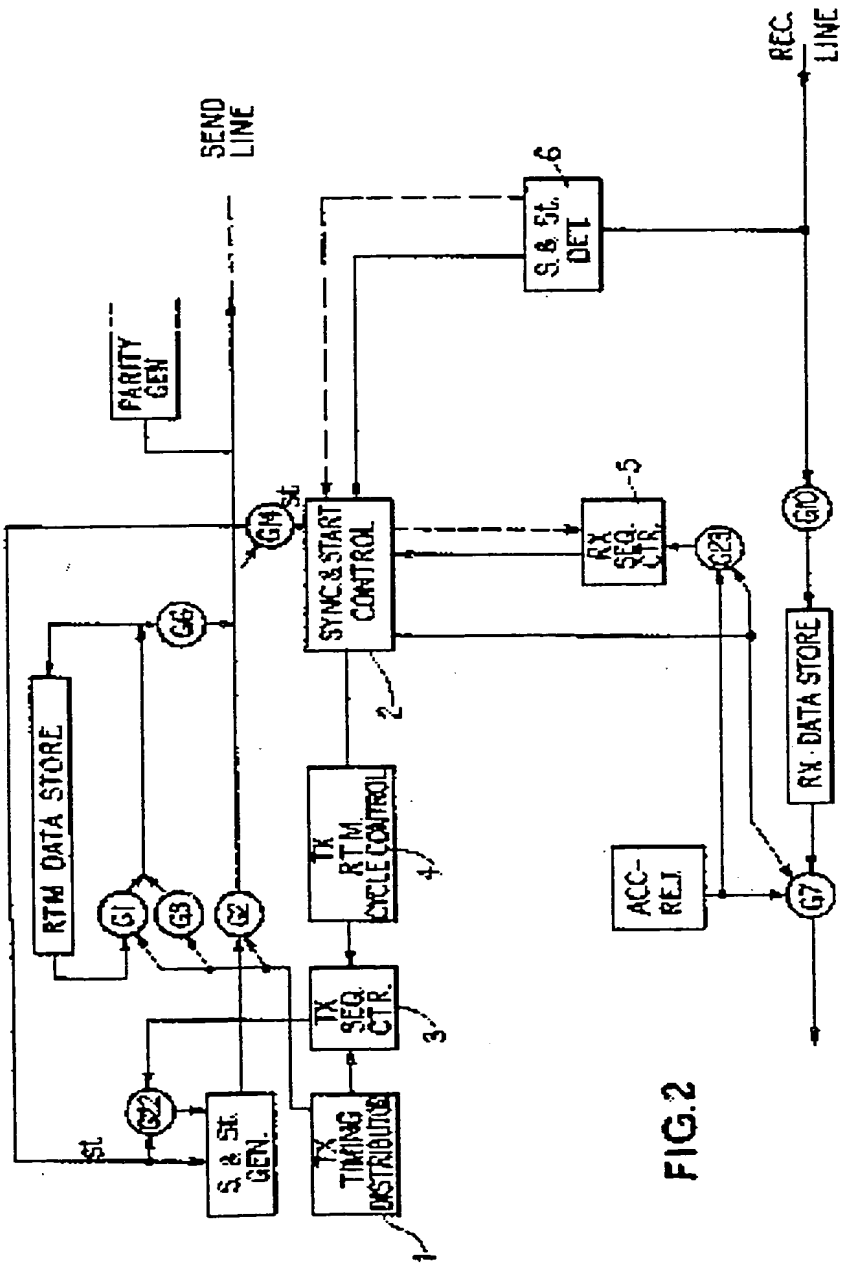

FIG.2